Oscilloscope Input Overload Detection: Project Executive Summary

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The purpose of this project was to design an overload detection circuit to be used on the analog front end of oscilloscopes developed and produced by Tektronix. This was a continuation of the previous work done by an engineer at Tektronix. The goal was to create a prototype circuit that detects when a user applies an input voltage that is too high and sends a signal to stop operation so that the oscilloscope is not damaged.

This project was done in partnership with Tektronix. It will be beneficial to them by replacing their current overload detection design which runs on a microcontroller and can sometimes be too slow. The overload detection for this project is an analog design that can detect overloads more quickly and can be calibrated more easily. It is intended to be used on their mainstream oscilloscopes.

This is strictly a hardware design project that avoided the use of any microcontrollers and embedded programming. The only involvement of a microcontroller is a signal sent to a control unit when an overload is detected. The input voltage cannot be measured directly since the measurement would introduce noise into the input line. Therefore, voltage overload is detected by correlation with temperature change.

The primary contributors to this project were the senior design group working on it for their Electrical and Computer Engineering capstone design class. The group consists of three members who are listed at the top of this document. The other contributors were employees of Tektronix, who provided advice, example schematics, and design tools.

The first phase of the project was research, which included understanding previous solutions and deciding which solutions will be best going forward. The project team met with the project partner weekly to plan logistics and get an understanding of the needs of the project and the design already completed. The second phase was design. The project was broken into several blocks that were assigned to different team members. All blocks were validated and reviewed by the instructors of the senior design course. The blocks were then individually tested with breadboarding and some small PCBs. With all blocks complete, the full system was laid out in PCB software, and simulated. The third phase was assembly and testing. The PCB was assembled in Tektronix facilities. Initial testing was complete with home equipment to get the calibration working at room temperature. Then, testing in Tetkronix’s temperature controlled chamber was completed. The final phase of the project is closeout, which includes making sure the project is well documented.

One important lesson learned from this project is the amount of simulation, testing, and tweaking that is required to work on an analog circuit design project. This required the team members to be knowledgeable about their assigned analog blocks and how changing different values would affect the output and behavior of the circuit. Another important lesson was that a project with a big project partner requires additional logistics in order to keep the project moving smoothly. This was in the form of NDAs and needing to coordinate times to commute and pick up necessary supplies from the project partner. This was a valuable lesson to learn and it was easy to work with Tektronix. They were accommodating with our needs as a capstone team.

The circuit will be handed off to Tektronix at the end of the project so that they can continue development or make any final tweaks and modifications prior to production use.

Protection Timeline	By Bradley Heenk, Calder Wilson, and Brandon Rawson			
Artifact	**Due Date**	**Task Breakdown**	**Parties Involved**	**Associated Meeting Time and Location**
1 Initial Project Development				
1.1 Project Assignments	Week 1	Receive assigned project		
1.2 Initial Project Partner Meeting	Week 2	Meet with Brian Mantel from Tektronix	Project Team, Brian Mantel	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams
1.3 Project Charter	Week 7	Revise executive summary, team communication protocols and standards, and risk register	Project Team	Weekly Mon. Team Meeting, 3 - 5 pm, Discord
		Create project timeline and engineering requirements summary		
		Compile all above items into project charter		
1.4 Final Engineering Requirements Draft	Week 9	Review feedback from engineering requirements draft	Project Team, Brian Mantel	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams
		Revise and confirm final requirements and testing plan		
		Submit changes on student portal		
		Send requirements to project partner		
1.5 Final Block Diagram Due	Week 10	Submit block diagram images and interface definitions through student portal	Project Team, Brian Mantel	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams
		Send copy to project partner		
2 Advanced Research and Building				
2.1 Block Validations	Week 13	Each team member completes design and validation of one block	Project Team	Weekly Mon. Team Meeting, 3 - 5 pm, Discord
2.2 First Block Checkoff	Week 14	Each team members proves that one of their blocks meets all interface properties	Project Team, TA	Fri. January 15th, 3:00pm - 5:00pm, Zoom
2.3 Design Reviews	Week 15	Sign up for slot and send project artifacts to peers	Project Team, Peer Reviewers	Thur. January 21st, 1:00pm - 3:30pm, Canvas
		Give presentation and review work of others		
		Send commented material's to peers		
2.4 Engineering Requirements Lock	Week 15	Engineers requirements are locked and cannot be changed after this date	Project Team, Brian Mantel	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams
2.5 Second Block Check-off	Week 17	Each team members proves that their second blocks meets all interface properties	Project Team, TA	Thur. Februray 4th, 3:00pm - 6:00pm, Zoom
2.6 Submit PCB Design for Fabrication	Week 17	Complete PCB design	Project Team, Brian Mantel	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams
		Have design review by project partner		
		Submit design for manufacturing		
3 Testing				
3.1 Final Block Check-off	Week 20	Each team members proves that their final blocks meets all interface properties	Project Team, TA	Weekly Mon. Team Meeting, 3 - 5 pm, Discord
3.2 Start and Complete PCB Assembly	Week 21	PCB should arive during week 19 and all parts should be available for manufacturing.	Project Team	Weekly Mon. Team Meeting, 3 - 5 pm, Discord
		Assemble multiple copies of the PCB to begin the testing phase.		
3.3 System Review 1	Week 24	Expected to show 8 of the 12 engineering requirements functioning on the system.	Project Team	Weekly Mon. Team Meeting, 3 - 5 pm, Discord
		The universal engineering requirement constraints must also be met for this system review.		
3.4 Charaterization Testing	Week 24	Using equipment provided by Tektronix, complete detailed testing of PCB	Project Team, Brian Mantel	Fri. May 12 pm - 5 pm, Tektronix, Beaverton
		Review results with project partner		
4 Project Presentation				
		Group submission of project materials and documentation.		
4.1 Completed Project Closeout Packet Draft Assignment	Week 26	Project closeout packet should be completed and in the peer review process.	Project Team	Weekly Mon. Team Meeting, 3 - 5 pm, Discord
		Used to finalize the achievements and goals of the project.		
4.2 Project Summary Video Assignment	Week 26	Requires a video outline before recording and the video should be 4 to 6 minutes long.	Project Team	Weekly Mon. Team Meeting, 3 - 5 pm, Discord
		Slides should be used to guide the video.		
		Video should be recorded after having the outline and slides reviewed.		
4.3 Final System Review	Week 27	Final verification that all engineering requirments are met	Project Team, TA	Mon. May 18, 4:00pm - 5:00pm, Zoom
4.4 Project Showcase	Week 27	Prepare quality packet of documentation that can be used to present the project.	Project Team	Thur. April 20 2:00pm - 3:00pm
4.5 Complete Documentation	Week 28	Ensure that documentation for Tektronix in format they require and up to their standards	Project Team, Brian Mantel	Weekly Mon. Partner Meeting, 2 - 3 pm, MS Teams